

67,200-571; TSMC 01-0249  
Serial Number 10/050,300

#### REMARKS

Favorable reconsideration of this application in light of the above amendments and the following remarks is respectfully requested.

Claims 9-18 are pending within this application. Claims 1-8 are canceled herein. Claims 17-18 are newly added herein. No claims have been allowed.

Paragraph 0042 is amended in part to correct a typographic error therein.

#### *Election/Restriction*

The Examiner has made FINAL within this application a restriction requirement under which applicant has previously elected prosecution of structure claims 9-16.

In response to the restriction requirement made FINAL, applicant cancels herein claims 1-8.

#### *Drawings*

The Examiner has objected to applicant's drawing figures 3, 4 and 5 as missing particular reference numerals (i.e., reference numeral 17 within figure 3 and reference numeral 20 within figures 4-5).

In response, applicant has amended applicant's drawing figures 3, 4 and 5 accordingly, to address the deficiency as cited by the Examiner. Replacement drawing sheets 1/2 and 2/2 are appended having contained therein corrected drawing figures 3, 4 and 5.

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***Specification***

The Examiner has objected to applicant's specification incident to inaccurate designation of reference numerals therein.

In response, applicant has amended applicant's specification accordingly at paragraph 0045, to address the deficiency as cited by the Examiner.

In light of the foregoing response, applicant respectfully requests that the Examiner's objection to applicant's specification be withdrawn.

***Claim Rejections — 35 U.S.C. § 103***

The Examiner has rejected claims 9-16 under 35 U.S.C. § 103(a) as being unpatentable over Farnsworth (U.S. Patent No. 6,555,460).

Applicant first notes that the Examiner at page 4, paragraph 2, characterizes Farnsworth's layer 1016 as a conductor passivation layer. Applicant next notes that the Examiner at page 5, paragraph 1 characterizes Farnsworth's microelectronic fabrication as an optoelectronic microelectronic fabrication. Applicant finally notes that the Examiner at page 4, paragraph 2 acknowledges that Farnsworth does not disclose a bond pad being formed from a conductor material selected from the group consisting of aluminum and aluminum alloys.

In response, applicant first notes that Farnsworth at col. 2, lines 48-52 characterizes Farnsworth's layer 1016 as a conductive repattern trace which is apparently intended as an extension of Farnsworth's bond pad, rather than a conductor passivation layer as an independent layer upon Farnsworth's bond pad, as disclosed and claimed by applicant within

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claim 9 and claim 13. Next, applicant notes that Farnsworth at col. 2, lines 8-10 discloses Farnsworth's invention as directed towards a flip-chip microelectronic fabrication, which is apparently not understood by a person skilled in the art as being an optoelectronic microelectronic fabrication, as disclosed by applicant and claimed within claim 13. Finally, applicant notes that Farnsworth at claim 18 and claim 19 discloses Farnsworth's bond pad, as well as Farnsworth's conductive repattern trace, as being formed comprising copper, nickel, palladium, platinum, gold or an alloy thereof which apparently teaches away from a bond pad formed of a conductor material selected from the group consisting of aluminum and aluminum alloy conductor materials, as disclosed by applicant and claimed within claim 9 and claim 13..

Thus, since each and every limitation within applicant's invention as disclosed and claimed at least in part within one of claim 9 and claim 13 is not disclosed within Farnsworth, in particular with respect to an optoelectronic microelectronic fabrication comprising a bond pad formed from a conductor material selected from the group consisting of aluminum and aluminum alloy conductor materials having formed thereupon a conductor passivation layer, applicant asserts that claim 9 and claim 13 may not properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Farnsworth.

Since all remaining claims within this rejection are dependent upon claim 9 or claim 13 and carry all of the limitations of claim 9 or claim 13, applicant additionally asserts that those remaining claims may also not properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Farnsworth.

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In light of the foregoing response, applicant respectfully requests that the Examiner's rejections of claims 9-16 under 35 U.S.C. § 103(a) as being unpatentable over Farnsworth be withdrawn.

#### ***Other Considerations***

Applicant has newly added claims 17-18 as directed towards a linewidth of applicant's conductor barrier layer being contained within a linewidth of applicant's bond pad. Support for newly added claims 17-18 is found within applicant's specification within paragraph 0042 as newly amended, which in turn finds support within applicant's figure 3, as originally filed.

The Examiner has cited no additional prior art of record not employed in rejecting applicant's claims to applicant's invention. No fee is due as a result of this amendment and response.

#### **SUMMARY**

Applicant's invention as disclosed and claimed within claim 9 and amended claim 13 is directed towards a microelectronic fabrication or an optoelectronic microelectronic fabrication comprising a bond pad formed of a conductor material selected from the group consisting of aluminum and aluminum alloy conductor materials, in turn having formed thereupon a conductor passivation layer. Absent from the prior art of record employed in rejecting applicant's claims to applicant's invention is a disclosure of each and every limitation within applicant's invention.

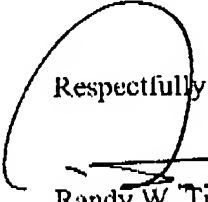
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### CONCLUSION

On the basis of the above amendments and remarks, reconsideration of this application, and its early allowance, are respectfully requested.

Any inquiries relating to this or earlier communications pertaining to this application may be directed to the undersigned attorney at 248-540-4040.

Respectfully submitted,

  
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